Code No: RT22023 **R13** SET - 1

II B. Tech II Semester Supplementary Examinations, Dec - 2015
PULSE AND DIGITAL CIRCUITS
(Com. to EEE, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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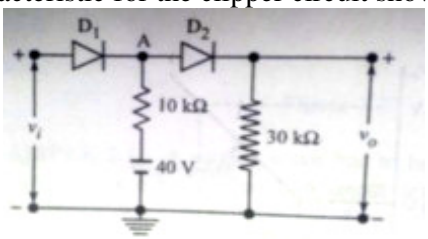
PART –A

1. a) Why a resistive attenuator is to be compensated? Also explain how is it compensated, (3M)
   b) State clamping circuit theorem. (3M)
   c) What is a non-saturated binary and what are its advantages when compared to a saturated binary. (4M)
   d) What are the merits and demerits of ECL? (4M)
   e) Define the terms slope error and displacement error. (4M)
   f) What is a sampling gate? Mention different types of them. (4M)

PART -B

2. a) Using relevant diagrams and wave forms explain the response of a high pass RC circuit to ramp input. Obtain the expression for its output voltage. (10M)
   b) Discuss in detail about diode storage and transition times. (6M)

3. a) Obtain the transfer characteristic for the clipper circuit shown in figure below. (10M)



   b) Explain the operation of a transistor clipper using relevant circuit diagram. (6M)

4. a) Design a monostable multivibrator with a gate width of 2 ms. (8M)
   b) Explain the operation an emitter coupled astable multi vibrator (8M)

5. a) Explain the operation of a 2 input NMOS NAND gate. (8M)
   b) Explain the operation of a CMOS NOR gate. (8M)

6. a) Explain the basic principles of Miller and Bootstrap time base generators. (10M)
   b) Define sweep time, fly back time. Derive transmission error in sweep circuits (6M)

7. a) Explain the synchronization technique with monostable multivibrator? (8M)
   b) Explain the mechanism of frequency division with astable multivibrator? (8M)

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